UM10072

ISP1564 eval board

Rev. 02 — 8 May 2007 **User manual**

Document information

Info	Content
Keywords	isp1564; usb; universal serial bus; host controller
Abstract	The ISP1564 eval board is a standard implementation of the ISP1564 in a complete configuration that allows you to exercise all signals and main features.

Revision history

Rev	Date	Description
02	20070508	Second release. Updated Fig 6.
01	20061212	First release.

Contact information

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1. Introduction

The ISP1564 evaluation (eval) board is a standard implementation of the ISP1564 in a complete configuration that allows you to exercise all signals and main features. Fig 1 shows the ISP1564 eval board.

Some of the features that are implemented in the ISP1564 eval board are:

- Selection between PCI V_{AUX} and PCI V_{CC} power supply, with voltage presence indicator. This feature together with the auxiliary +5 V input on J1 allows you to test the system wake-up from power management states, such as $S3_{cold}$, in which PCI V_{CC} is not present. This is intended mainly to test the ISP1564 in motherboard or notebook designs.
- Simple and reliable overcurrent protection scheme that allows testing of the OCn_N and PWEn_N signals. Alternative solutions, resettable circuit protection devices, can be adopted.
- Port power LEDs that may be omitted in a standard commercial implementation but are considered useful on the eval board for easier understanding of functionality and debugging.
- System tuning selection jumper, allowing quick and early assessment of final system setting requirement.

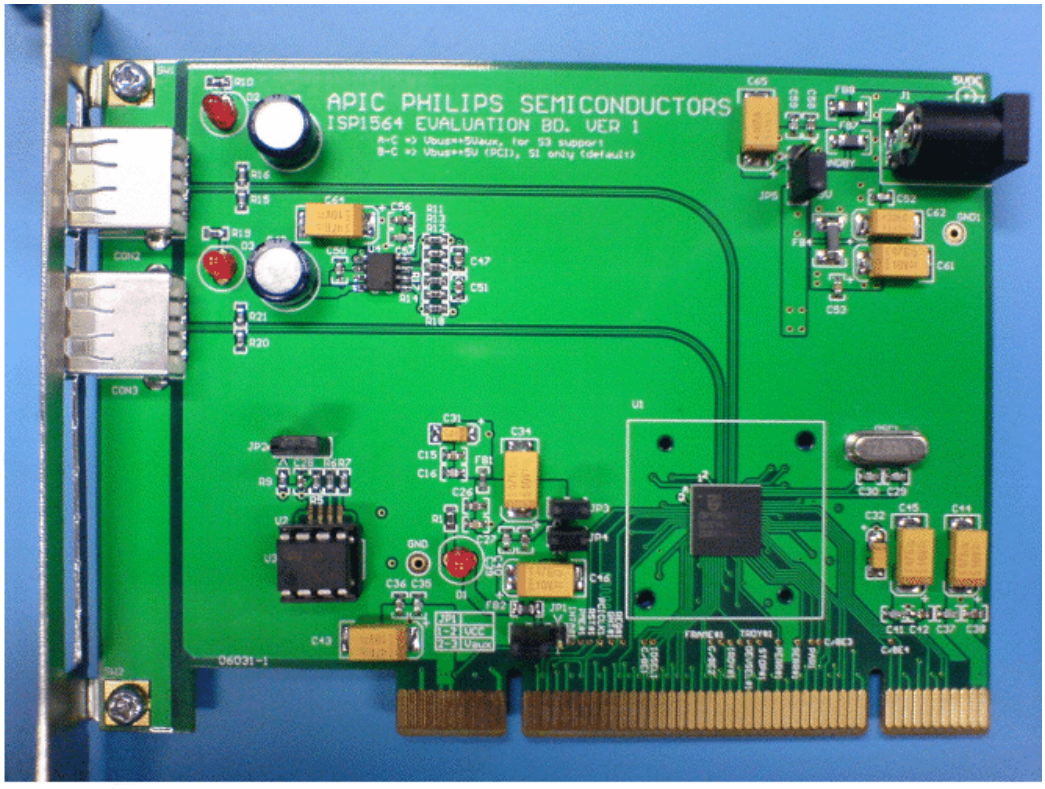
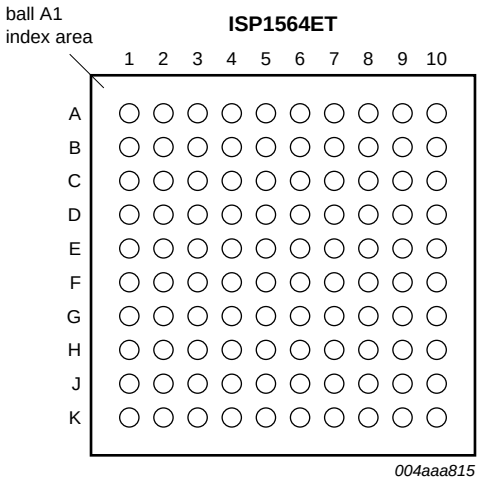


Fig 1. ISP1564ET eval board

2. ISP1564 pin configuration



Transparent top view

For details on the ball assignment, refer to the ISP1564 data sheet.

Fig 2. Pin configuration

3. System requirements

- Intel PII400 MHz processor and above, or equivalent in speed from AMD, Cyrix and VIA is recommended.

  Remark: Only motherboards with 3.3 V PCI interface can be used with the ISP1564 eval board.

  Generally, the processor usage indicator varies depending on the type and number of applications launched to exercise attached USB devices. For example, running data transfer tests on two high-speed HDDs on a P4 at 1.7 GHz, 128 MB DDRAM, Microsoft Windows 2000 will determine a processor usage of 30 % to 40 %. Adding two Original USB cameras and an application playing an MP3 song through Original USB speakers may increase the average processor usage up to 70 % to 80 %. Also, a Hi-Speed USB camera and an Original USB camera running simultaneously will increase the processor usage up to 100 %, depending on resolution settings.
- Motherboard with PCI slots that are compatible with *PCI Local Bus Specification Rev. 2.2;* supporting at least S1 and S3 power management modes for power management features testing.
- Memory: Minimum amount as indicated by the operating system and applications requirements. Only a small amount of memory is occupied by the installation of the device drivers itself, or the OHCI or EHCI functionality.
- HDD space: Mainly determined by the operating system and applications requirements because specific drivers need very little space.
- Graphics cards and other adapter cards: No special requirements.
- Operating systems supported: Windows 98 Second Edition (SE), Windows 2000, Windows XP and Windows Millennium Edition (Me). In Windows 98 SE, a separate EHCI driver is required for the high-speed USB functionality.

4. ISP1564 eval board

Fig 3 shows the eval board drawing.

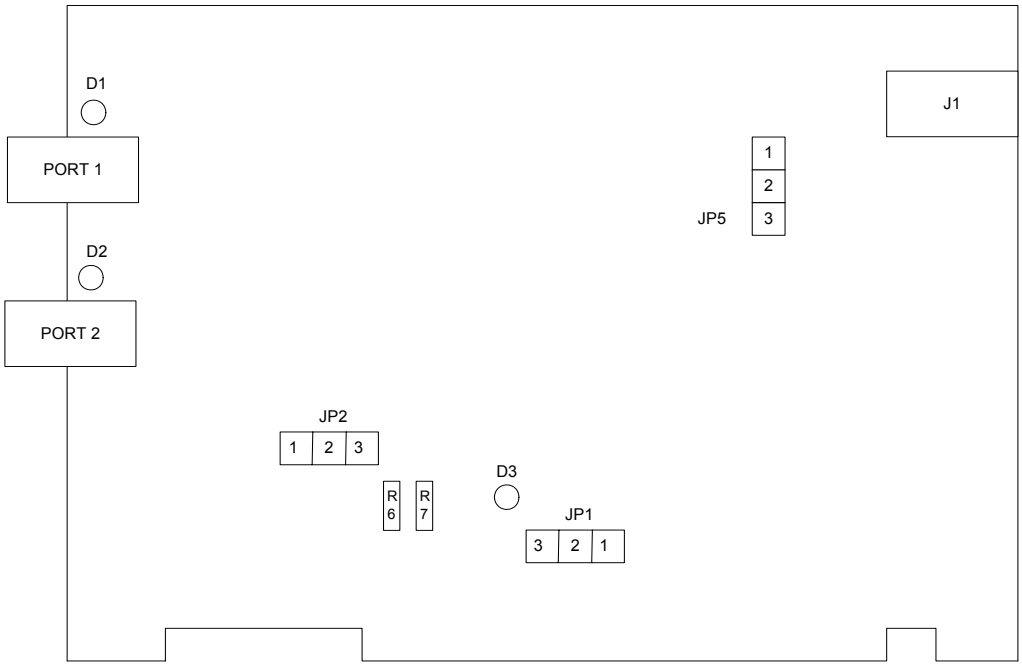


Fig 3. Eval board drawing

4.1 Port powered LEDs

LEDs D1 and D2 indicate the power status of USB ports. If a port is powered, the respective LED is turned on. It is turned off during system boot-up until OHCI or EHCI drivers are loaded, or it is switched off whenever an overcurrent condition occurs.

4.2 PCI V_{AUX} power supply

If the motherboard used is PCI 2.2 compliant, jumper JP1 position 2-3 can be shorted, allowing $S3_{cold}$ suspend and resume testing (PCI V_{AUX} = 3.3 V is used and an external +5 V is necessary). If the motherboard used is PCI 2.1 or older version compliant, jumper JP1 position 1-2 must be shorted (PCI V_{CC} = 3.3 V is used because PCI V_{AUX} is not present). Note that in both these situations, LED D3 must be turned on, indicating that the ISP1564 is powered.

Important*:* If LED D3 is not lit, when JP1 is in 2-3 position, it indicates that the ISP1564 does not have the PCI V_{AUX} supply; PCI V_{AUX} is not supplied in the PCI connector. Therefore, your computer will stop responding or ‘hang’ when the operating system is loading OHCI or EHCI drivers. Switch JP1 to position 1-2 to connect to PCI V_{CC} = 3.3 V, present under normal conditions, except some system power management modes. For example, $S3_{cold}$ and S4.

4.3 External 5 V power source and S3 wake-up

Jack J1 is used to connect an external +5 V standby power supply to test the system wake-up from $S3_{cold}$ and maintain the connected USB devices powered to avoid re-enumeration.

When the system is in the $S3_{cold}$ power management state, the +5 V main power at PCI connectors disappears. Therefore, all downstream ports will not be powered because V_{BUS} is derived from the PCI +5 V power supply. In this situation, downstream bus-powered devices, such as mouse and keyboard, are not functional and cannot wake up the system.

If you want to use the external +5 V supply, pins 1 and 2 of JP5 on the eval board must be shorted with a jumper cap. Similarly, if you intend to use PCI +5 V as only the V_{BUS} power source (no testing of the system wake-up from $S3_{cold}$ and no external +5 V connected), pins 2 and 3 must be shorted with a jumper cap. The use of jumper allows you to quickly change the V_{BUS} source selection.

4.4 Loading subsystem ID and vendor ID from external EEPROM

Expansion board vendors can use the subsystem vendor ID and the subsystem ID to identify the board and to load correct drivers by the operating system. The PCI-SIG assigns the subsystem vendor ID and the vendor determines the subsystem ID.

The subsystem vendor ID and the subsystem ID can optionally be loaded at power-on from the external serial I^2C-bus EEPROM present on the ISP1564 eval board. A 3.3 V serial EEPROM of any size can be used because only a few locations will be used for data loading.

An example on the I^2C-bus EEPROM programming is given in Fig 4. In the example, it is assumed that the subsystem vendor ID is 1132h, the subsystem device ID for OHCI is 1664h, and the subsystem device ID for EHCI is 1665h.

Address	I^2C-bus EEPROM content	
0	32h	Subsystem vendor ID LOW
1	11h	Subsystem vendor ID HIGH
2	64h	Subsystem device ID (OHCI) LOW
3	16h	Subsystem device ID (OHCI) HIGH
4	65h	Subsystem device ID (EHCI) LOW
5	16h	Subsystem device ID (EHCI) HIGH
6	FFh	reserved
7	15h(1)	reserved

(1) Loads subsystem vendor ID and device ID. For details, refer to the *ISP1564 Hi-Speed USB PCI host controller* data sheet.

Fig 4. I^2C-bus EEPROM programming example

Remark: Do not load any other values in reserved fields, otherwise, functionality of the ISP1564 is not guaranteed.

The default configuration of the eval board is with EEPROM access disabled. To use the EEPROM, resistors R6 and R7 must be removed.

4.5 Programming of the external EEPROM through PCI

To simplify the manufacturing procedure of the expansion board manufacturer, the ISP1564 has a feature using which the external EEPROM may be programmed in-circuit through the PCI bus. This feature is accomplished using the programming interface

described in Appendix I of *PCI Local Bus Specification Revision 2.2*. Note that the data structure described in Appendix I is not used.

VPD registers start from offset E4h of EHCI Host Controller's configuration registers.

Accompanying the eval board is a sample program that can demonstrate the ability to change subsystem vendor and device IDs.

4.6 System tuning for the ISP1564

To increase throughput of the USB transfer, the ISP1564 employs certain mechanisms. For details, refer to Section 11.4 of the ISP1564 data sheet. On some systems in which the PCI bus is congested, however, the ISP1564 may encounter buffer underrun (for OUT) and overrun (for IN) conditions during transfers.

These buffer underrun and overrun conditions may cause further reduction in throughput, in addition to that resulted from the congested PCI bus, causing the ISP1564 to operate in an unstable manner.

The ISP1564 has provisions for these mechanisms to be disabled using either EHCI operational register address 6Ch (for details, refer to Section 11.4 of the ISP1564 data sheet) or an external pin.

These mechanisms can also be disabled using system tuning setting jumper JP2 on the ISP1564 eval board. Shorting pins 1 and 2 of JP2 will disable these mechanisms, and shorting pins 2 and 3 of JP2 will enable them.

5. Hi-Speed USB (EHCI) drivers

For Windows 2000 SP4 or later, and Windows XP SP1 or later, the standard Microsoft EHCI drivers can be used. You can download the latest service pack corresponding to the specific operating system from the Microsoft website.

6. Schematics

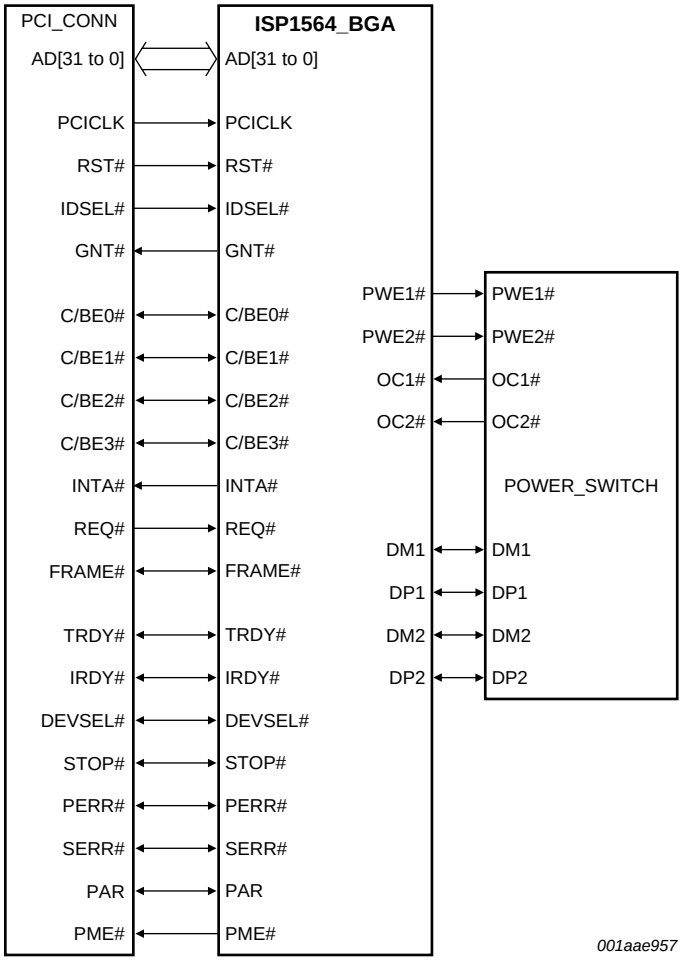


Fig 5. ISP1564 eval board – part 1

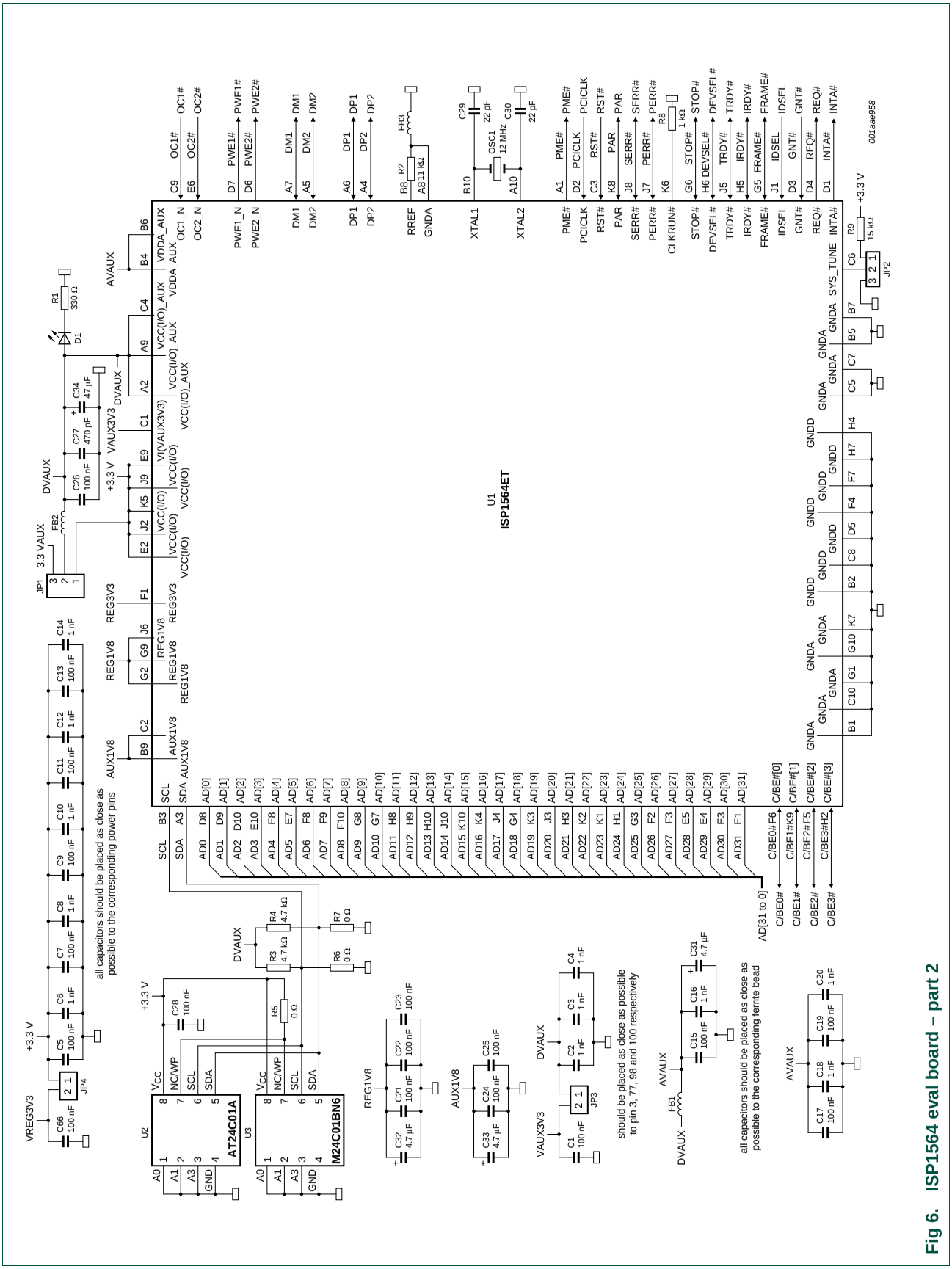


Fig 6. ISP1564 eval board – part 2

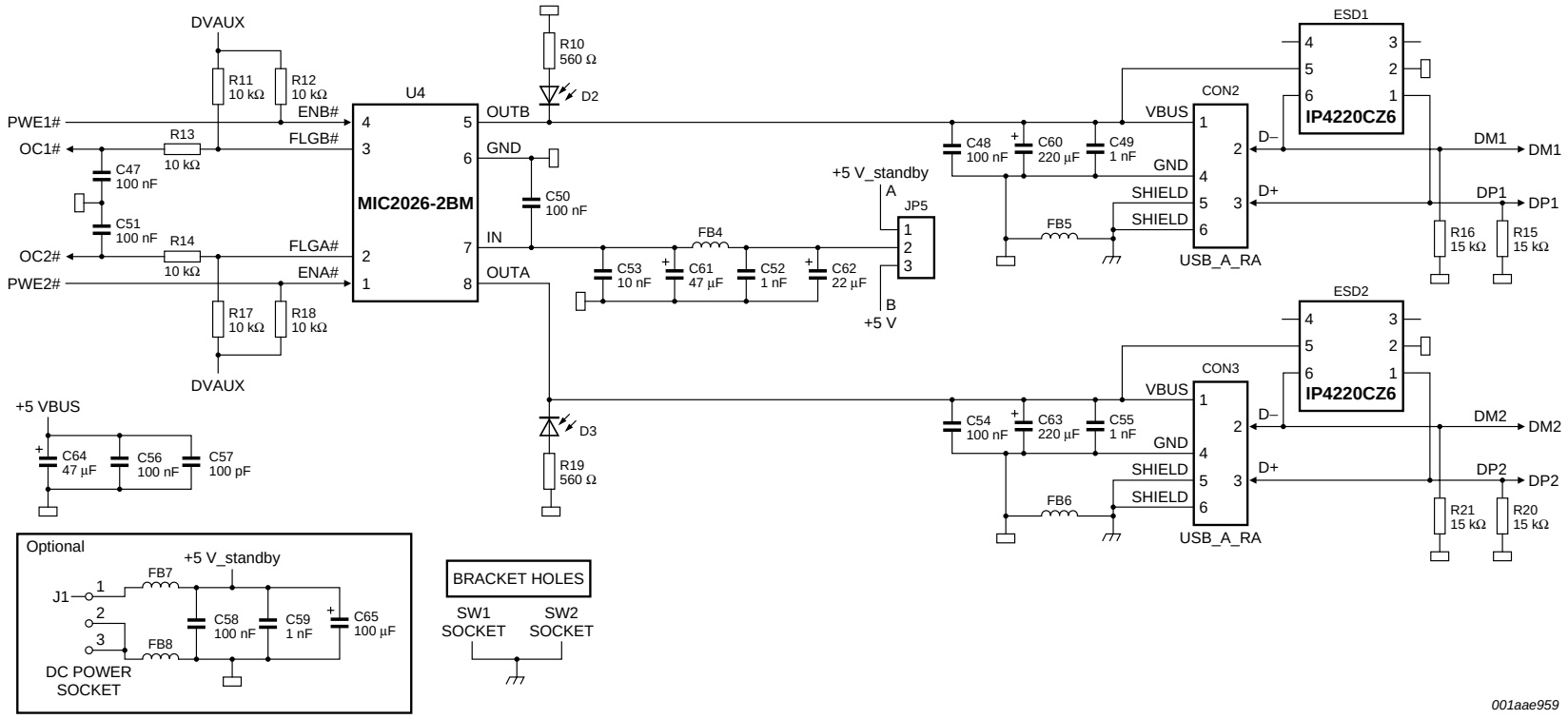


Fig 7. ISP1564 eval board – part 3

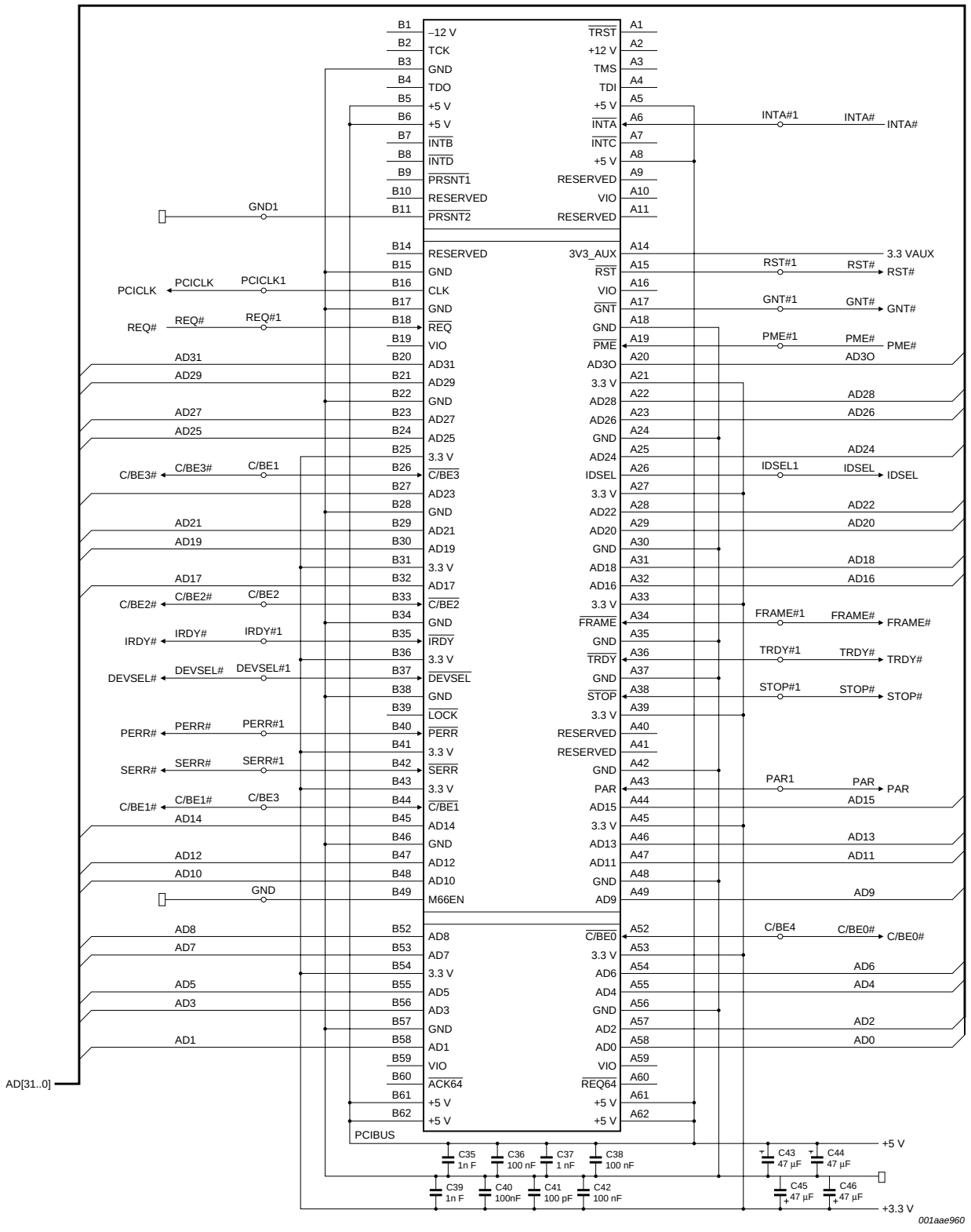


Fig 8. ISP1564 eval board – part 4

7. Bill of materials

Table 1. Bill of materials

Designator	Footprint	Part type
R5 R6 R7	0603R	0 Ω
C2 C3 C4 C6 C8 C10 C12 C14 C16 C18 C20 C35 C37 C39 C49 C52 C55 C59	0603C	1 nF
C1 C5 C7 C9 C11 C13C15 C17 C19 C21 C22 C23 C24 C25 C26 C28 C36 C38 C40 C42 C47 C48 C50 C51 C54 C56 C58 C66	0603C	0.1 µF
R8	0603R	1 kΩ
C53	0603C	10 nF
R3 R4	0603R	4.7 kΩ
C31 C32 C33	CASE-A	4.7 µF
R11 R12 R13 R14 R17 R18	0603R	10 kΩ
R2	0603R	11 kΩ / 1 %
OSC1	XTAL1	12 MHz
R9 R15 R16 R20 R21	0603R	15 kΩ
C29 C30	0603C	22 pF
C62	CASE-C	22 µF / 10 V
C34 C43 C44 C45 C46 C61 C64	CASE-D	47 µF / 10 V
C41 C57	0603C	100 pF
C65	CASE-D	100 µF / 10 V
C60 C63	REC15/3	220 µF / 10 V
R1	0603R	330 Ω
C27	0603C	470 pF
R10 R19	0603R	560 Ω
U3	DIP8	AT24C01A-2.7
U2	SO8	AT24C01A-2.7
FB1 FB3 FB5 FB6	0603G	BLM18PG121SN1
FB2	0805G	BLM21PG221SN1
FB7 FB8	1206	BLM31PG121SN1
FB4	1206Cust	BLM41PG600SN1
JP1 JP2 JP5	SIP3	HEADER 3

Designator	Footprint	Part type
JP3 JP4	SIP2	HEADER 2
ESD1 ESD2	SO6CUST	IP4220CZ6
U1	TFBGA100	ISP1564ET
J1	DC JACK2	JACK
D1 D2 D3	LED3	LED
U4	SO-8	MIC2526
SW1 SW2	M-HOLE2	SOCKET
CON2	USB-TYPEA	USB 1
CON3	USB-TYPEA	USB 2

8. Abbreviations

Table 2. Abbreviations

Acronym	Description
DDRAM	Double Data Random Access Memory
EHCI	Enhanced Host Controller Interface
HDD	Hard Disk Drive
OHCI	Open Host Controller Interface
PCI	Peripheral Component Interconnect
USB	Universal Serial Bus

9. References

- ISP1564 Hi-Speed USB PCI host controller data sheet
- Designing a USB 2.0 Host PCI Adapter Using ISP1564 application note
- Universal Serial Bus System Architecture, First and Second Editions from MindShare
- Universal Serial Bus Specification Rev. 2.0
- PCI Local Bus Specification, Rev. 2.2
- PCI Bus Power Management Interface Specification, Rev. 1.1
- PCI System Architecture, Fourth Edition from MindShare

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11. Contents

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